 **Khulna University of Engineering & Technology**

Department of Computer Science and Engineering

**Project Report**

Submitted By

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**Topic** : 21 bit Mini computer design using Logisim.

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**Course Name** : Computer Architecture

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**Objectives**:

* To develop a minimal computer system using “Logisim” software, along with components like central processing unit (CPU) and a main memory.
* To learn implementation of ALU, registers, instruction set architecture, MAR, MBR, IR, control unit, CPU and main memory (RAM) in minimal computer system.
* To implement various instructions like AND, OR, NOR, BRANCH,LOAD,SOTRE,ADD,SUB,MUL & HALT.
* To understand how an instruction is fetched to a computer and how it functions internally.

**Introduction:**

Introducing the small computer system we have: including a wealth of important instructions, like branch, stop, add, sub, load, store, mul, and and. It consists of important parts including the control unit, CPU, main memory, MAR, MBR, IR, ALU, and accumulators in addition to complex algorithms like Booth's Algorithm. Designed with customization and efficiency in mind, it offers powerful features

|  |  |
| --- | --- |
| **Component** | **Description** |
| Word Size | 21 bits |
| OP-Code | 4 bits |
| RAM Address Size | 12 bits |
| Architecture | 21-bit architecture with 12-bit RAM addressability |

**Instruction Format:** (21 Bits)

|  |  |  |
| --- | --- | --- |
| **Don’t Care** | **Op-Code** | **Memory Address** |
| 5 bits | 4 bits | 12 bits |

**Instruction set with opcode**:

0 – AND : perform logical and operation between two operands.

1 – ADD : perform addition between two operands.

2 – STORE : store the result of the operation in memory.

3 – OR : perform logical OR between two operands.

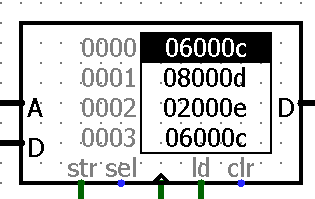
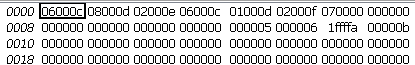
4 – SUB : perform subtraction between two operands.

5 – BUN : branch unconditionally.

6 – LDA : loads data from memory to accumulator.

7 – HLT : halt the CPU.

**Sample program:**



**Discussion:**

The CPU stores both data and instructions in the same memory, using the simple Von Neumann architecture. Only a few simple tasks are carried out here. A single clock pulse is used to complete each action. The Logisim simulator has all of these designs implemented. Every arithmetic and logical action on data kept in registers is handled by the CPU's ALU. ALUs that can execute addition, subtraction, AND, OR, and multiplication can be designed with the help of Logisim's tools. The data and instruction flow inside the CPU is regulated by the control unit. Our system provides enough of storage and memory access capabilities with a 12-bit RAM addressability and a 21-bit accumulator. Depending on whatever instruction is being executed at the time, it regulates how other CPU components operate.